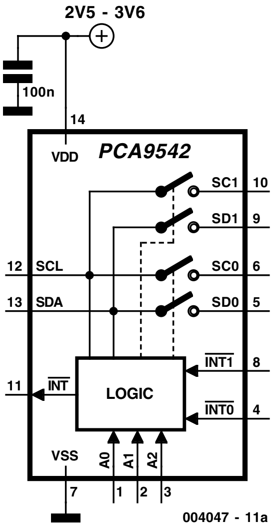
046

I²C Multiplexer



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Anyone who wants to build large I²C bus structures sometimes has the problem that the four or eight addresses of a particular type of IC are not sufficient, or that the capacitive loads on the SDA and SCL lines are very high, so that a low clock frequency must be chosen for the bus. The multiplexer ICs described here allow a large I²C bus system to be partitioned into several zones. These ICs connect the I²C bus controller to the zone that is to be addressed at any given time.

It can also happen that parts of the I²C bus must be operated at 3 V, while other parts must be operated at 5 V. The multiplexers are also helpful here, since their inputs and outputs can both be loaded with 5-V signals, even though the multiplexer operates with only +3 V. The PCA9542 and PCA9544 ICs (**Figure 1**) contain 1-to-2 and 1-to-4 multiplexers, respectively, for both of the bidirectional SDA and SCL lines. These ICs can be operated from supply voltages between 2.5 and 3.6 V (3 V nominal). When operating power is first applied to the multiplexer IC, the attached I²C 'islands' are initially isolated, since the multiplexer is in a high-impedance state. The IC must first be accessed using its own I²C address and a control byte, in order to allow one of the two or four attached I²C line pairs to be connected through to the main I²C bus. In order to avoid interference to data transfers on the I²C bus, the connection is made only after the following Stop state, when the bus is again free.

Each of the multiplexer ICs has three address pins (A0, A1 and A2), so up to eight PCA954x ICs can be operated in parallel. Provisions are also made for handling interrupts. Each of the I²C zones has its own interrupt line, and all of the lines for the various zones are coupled in an AND arrangement. The I²C bus of the zone that is the source of the interrupt does not have to be actively connected to the main bus. The summed interrupt signal arrives at the interrupt input of the controller via an open-drain output. The controller detects that an interrupt has been generated somewhere in the overall system, and it must then determine the source zone of the interrupt by polling the multiplexers (by reading out their control bytes). After this, it can poll the ICs in the identified zone. The interrupt line of the I²C bus is released only after the IC that triggered the interrupt has been accessed and the interrupt has been acknowledged. If other interrupts have been generated in the meantime, the interrupt line will remain Low, and the controller must again search for the IC(s) that triggered the interrupt(s).

Figure 2 shows an example of an I²C bus system with one part that works at +3 V and a second part that is wired with +5-V pull-up resistors. Note that the pull-up resistors between the controller and the PCA9542 multiplexer are necessary to allow the multiplexer to be initially accessed after the 3-V supply voltage comes up, when it is still in the isolating state. If these resistors have larger values than the pull-up resistors used in the 5-V zones (by a factor of ten), the voltage in the +5-V zones will be able to rise to an adequate level.

The PCA9542 comes in a TSSOP-14 package, while the PCA9544 comes in a TSSOP-20 package. Additional information can be found at www.semiconductor.philips.com.

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